REMARKS

Claims 1-23 are pending in this application. By this Amendment, claim 1 has been amended to correct an informality. Thus, no new matter is added by this Amendment.

I. Claim Objections

The Office Action objected to claim 1 because the recitation "the linked packet" has no antecedent bases. To this end, Applicant amend claim 1 to recited "a write circuit which links each received packet with the generated identification information, and writes the received packet and identification information into a packet storage memory." Applicants submit the requirements of the Patent Office have been met.

II. Rejections Under 35 U.S.C. §103(a)

A. Lawande in view of Fujimori

Claims 1, 3, 10-12, 14-15, 17-18, 20-21 and 23 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,219,697 (hereinafter "Lawande") in view of U.S. Patent No. 6,108,718 (hereinafter "Fujimori"). This rejection is respectfully traversed.

The present invention is directed to determining whether or not a reset occurred between the reception of one packet and the next packet, by checking for a change in the one packet and the next packet identification information. More specifically, the present invention as recited in claim 1 is directed towards a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, and a write circuit which links each received packet with the generated information and writes the received packet and identification information into a packet storage memory. This procedure, and the associated benefit, of determining whether or not the packets received in different reset intervals is nowhere taught by Lawande.

The Patent Office acknowledges that Lawande fails to teach a circuit which generates identification information for determining whether or not one received packet and the next received packet are received during different reset intervals. The Patent Office cites Fujimori as curing this deficiency. Applicants respectfully disagree.

Under the IEEE 1394, when a bus reset occurs, topology information relating to nodes is cleared and physical addresses are re-allotted. For example, as shown in Fig. 6 of Fujimori, when a new device 12 is connected to the IEEE 1394 and a bus reset occurs, re-allotting of physical addresses starts so that physical addresses are re-allotted to the new device 12. Thus, physical addresses of the devices 11 and 13 are changed. If a bus reset occurs while the device 14 is transferring data to the device 13, the device 14 will lose physical addresses of the device 14 (which is the destination address of the data transfer) after the bus reset.

In order to solve the above-identified problem, Fujimori devises a system which finds the device 14 by transferring a command to all the devices with a broadcast transfer after a bus reset (see Fig. 7A).

Fujimori is directed to sending a command to find a device after a bus reset. Moreover, Fujimori is directed to distinguishing devices before a bus reset from devices after a bus reset, but not packets before a bus reset from packets after a bus reset.

The claims of the present invention, however, are directed to determining whether a received packet is a packet received before or after a reset. For example, according to an embodiment of the present invention, the firmware can learn the place at which resets occurred (boundaries of received packets in the packet storage memory) by checking identification information (BT). See Fig. 10 of the present application.

Fujimori is silent regarding a circuit which generates the above identification information and regarding writing a linked packet and identification information into a packet storage memory. Further, Fujimori does not disclose a register which stores a pointer

distinguishing a received packet area before a reset from a received packet area after a reset (see Fig. 12 of the present application). Moreover, Fujimori does not disclose a register which stores status information indicating that the transmission of a packet by a transmission start command has been halted by a reset (see Figs. 17A to 17D, 25 and 26). See page 24, lines 6-35 of the specification of the present application. In other words, Fujimori fails to teach or suggest a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, and a write circuit which links each received packet with the generated information and writes the received packet and identification information into a packet storage memory, as recited by claim 1.

Thus, Fujimori does not cure the deficiencies of Lawande.

With respect to amended claim 10, nowhere does Lawande teach or suggest a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, as recited in claim 10.

More specifically, claim 10 recites a data transfer control device for transferring data between a plurality of nodes connected to a bus, wherein the data transfer control device comprises a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, a link circuit which provides services for transmitting read packet to each node, and a status storage register which stores status information indicating that the transmission of a packet has been halted, when the transmission of the packet has been halted by the occurrence of a reset that clears node topology information.

In other words, as supported by the specification at, for example, Figs. 17A-17D, if a reset occurs slightly before the transmission start command has been issued, the processing section cannot determine which of the cases has occurred and thus the processing stalls (see

Figs. 17B and 17C). However, the status storage register stores status information indicating that the transmission of a packet has been halted due to the occurrence of a reset (see Fig. 17D). Therefore, the present invention, as defined by claim 10, allows the processing means to easily distinguish the cases (see step S41 of Fig. 18), thus preventing the processing of the processing section from being stalled. See page 34, line 2 to page 35, line 27 of the specification.

Lawande merely teaches an interrupt to indicate the entry into Bus Reset. See col. 12, lines 53-54 of Lawande. Existing TCP connections between nodes, other than the node being inserted/removed, are not reset upon entering the Bus Reset state. See col. 12, lines 61-63.

Nowhere does Lawande teach or suggest a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, as recited in claim 10. Nowhere does Lawande teach or suggest the status storage register which stores status information indicating that the transmission of a packet has been halted, when the transmission of the packet has been halted by the occurrence of a reset that clears node topology information, as recited in claim 10. This benefit allows prevention of stalls, for example, in the processing of the hardware, even if a reset occurs slightly before the issue of a transmission start command. This benefit is nowhere taught or suggested by Lawande.

Further, nowhere does Fujimori cure this deficiency.

For the foregoing reasons, Applicants respectfully submit that Lawande fails to teach or suggest the subject matter of independent claims 1 and 10 or any of depending claims 3, 11, 12, 14, 15, 17, 18, 20, 21 and 23. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Lawande in view of Fujimori and further in view of Robins

Claim 2 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lawande in view of Fujimori and further in view of U.S. Patent No. 5, 590, 124. This rejection is respectfully traversed.

Claim 2 depends from claim 1 and adds that the identification information is a toggle bit that toggles from zero to one or from one to zero when one received packet and the next received packet are packets received within different reset intervals.

The Patent Office acknowledges that Lawande and Fujimori fail to teach identification information but that it would have been obvious to one of ordinary skill in the art at the time of the invention that a toggle bit is a common status indicator. However, even if one of ordinary skill in the art would have found Robins to teach a toggle bit to indicate the status of a pin, as alleged by the Patent Office, the currently claimed invention still would not have been achieved. That is, nothing in Lawande, Fujimori, and/or Robins teach or suggest a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, and a write circuit which links each received packet with the generated information and writes the received packet and identification information into a packet storage memory, as recited by claim 1.

For the foregoing reasons, Applicants submit that claim 2 is thus allowable for the same reasons as claim 1, as discussed above. Reconsideration and withdrawal of the rejection are thus respectfully requested.

C. Lawande in view of Gehman

Claims 4-9, 13, 16, 19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lawande in view of U.S. Patent No. 6,304,553 (hereinafter "Gehman"). This rejection is respectfully traversed.

As acknowledged by the Patent Office, Lawande does not teach a first pointer storage means for storing pointer information that specifies a boundary in the package storage means. However, the Patent Office alleges that Gehman teaches a data transfer control device where pointer information specifies a boundary in storage.

The Patent Office referenced col. 5, lines 48-59 of Gehman where it is stated "the removal is accomplished by storing or remembering the FIFO right pointer location before writing the 1394 header."

Claim 4 recites a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory between an area for a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset. The configuration recited in claim 4 allows avoidance of hardware processing stalls by enabling preferential processing of a packet received after the reset has occurred.

Specifically, as shown in Fig. 12 of the present application, the first pointer information storage register BPR stores first pointer information BP that specifies a boundary RBI in the packet storage memory between an area of a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset. In this way, the processing section (firmware) may easily distinguish a packet received before the occurrence of a reset from a packet received after the occurrence of the reset, and thus reducing a processing load on the processing section (see Fig. 13B and 13C). See page 28, line 1 to page 34, line 1. This benefit is nowhere taught by Lawande or Gehman, alone or in combination.

Nowhere do Lawande and Gehman teach or suggest a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory for an area for a packet received before the occurrence of the reset that clears node topology

information and an area for a packet received after the occurrence of the reset, as recited in claim 4.

Further, Lawande and Gehman, alone or in combination, fail to disclose a second pointer storage register which stores second pointer information that specifies a boundary in the packet storage memory between an area for processed packets and an area for unprocessed packets, and a third pointer storage register which stores third pointer information which specifies a boundary in the packet storage memory between an area for received packets and an area storing no received packets, as recited in claim 6.

Still further, Lawande and Gehman, alone or in combination, fail to disclose a fourth pointer storage register which stores fourth pointer information which specifies a boundary in the control information area between control information for a packet received before the occurrence of the reset that clears node topology information and control information for a packet received after the occurrence of the reset, and a fifth pointer storage register which stores fifth pointer information which specifies a boundary in the data area between data of a packet received before the occurrence of the reset that clears node topology information and data of a packet received after the occurrence of the reset, as recited in claim 8.

Accordingly, Applicants respectfully submit that Lawande and Gehman, alone or in combination, do not teach or suggest the features of independent claim 4, depending claims 6 and 8 or any of depending claims 5, 7, 9, 13, 16, 19 and 22. Reconsideration and withdrawal of this rejection are thus respectfully requested.

III. Dependency of Claims 18-23

Claims 18-23 were incorrectly construed by the Patent Office to be independent claims. The Examiner asserts that a fee of $516.00 is owed for payment of the alleged six new independent claims.

Applicants submit that claims 18-23 are proper dependent claims and thus no additional fees should be due. Each of these claims refers to an earlier claim, thereby depending from and further limiting such claim. If the Examiner disagrees, Applicants respectfully request that the Examiner specifically state what defect, if any, the dependent claims have, or why they should otherwise be construed to be independent claims. In the absence of any reasoning provided by the Patent Office, Applicants submit this statement of the claims being independent claims should be withdrawn.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-23 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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